High speed and low power Hybrid carry skip adder using DMFA

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***Abstract*— The Adders are the integral part of the arithmetic and logic unit, hence increasing the performance of an adder is very important [1]. The Hybrid carry skip adder has better speed and less power utilization compare to conventional adders. In the modified carry skip adder, higher speed is achieved by concatenation and incrimination techniques. In addition, multiplexer in the skip logic of Conventional CSKA are replaced by use of AND-OR-Invert and OR-AND-Invert logic [3]. Then Hybrid CSKA using dual mode full adder (DMFA) is designed, which will replace the chain of ripple carry adders (RCA) present in the Hybrid carry skip adder with DMFA and Parallel prefix networks such as Brent-kung is used as a middle of the stage to achieve higher speed. The Proposed hybrid CSKA structure is analyzed by comparing the parameters of power, speed and area with a conventional carry skip adder and modified carry skip adder using 180 nm CMOS technology. Finally, ASIC implementation of Hybrid carry skip adder using DMFA is carried out by cadence Encounter tool and it start from pad creation, floor planning, power planning, placement and routing of designed Standard cell.**

***Index Terms*— carry skip adder (CSKA), high speed, low power, Hybrid carry skip adder, Parallel Prefix adders (PPA), DMFA.**

I. INTRODUCTION

Adders are the basic building blocks for any applications in arithmetic and logic unit. In ALU, the important role of an adder is addition operation and also in many other arithmetical operations. Hence designing of efficient adder is necessary for increasing performance in an ALU and it is also important for processors design [4]. The speed of the adders operation is increased through by carry propagation. For the implementation of an efficient adder, the carry which is generated in the each stage will be propagated to the output as early as possible, which will reduces the worst case path delay and it also finds the final speed of the digital circuits. The Hybrid carry skip adder has more speed and lower power utilization compared to the conventional adders. The speed enhancement of the carry skip adder is achieved by concatenation and incrimination techniques for improving the efficiency of the conventional adders. The multiplexer's logic in Conventional CSKA replaced by AND-OR-Invert and OR-AND-Invert logic gates for the designing skip logic. These adders can be designed for both fixed and variable stage. Finally, a hybrid carry skip is designed by using different Parallel Prefix adders (PPA), which reduces the power consumption without affecting the impacting of speed. The dual mode full adders (DMFA) are used in Hyb-CSKA to replace the Ripple carry adders which will reduce the power consumption than other proposed structures. The proposed hybrid carry skip adders are assessing by compare with their speed, delay and energy parameters with other adders [2].

II. DESIGN OF HYBRID CARRY SKIP ADDER

A. conventional carry skip adder

The carry skip adder (CSKA) uses skip logic to propagate the carry generated in each stage to next stage for speed up addition operation [4]. The figure.1 shows the architecture of conventional CSKA.

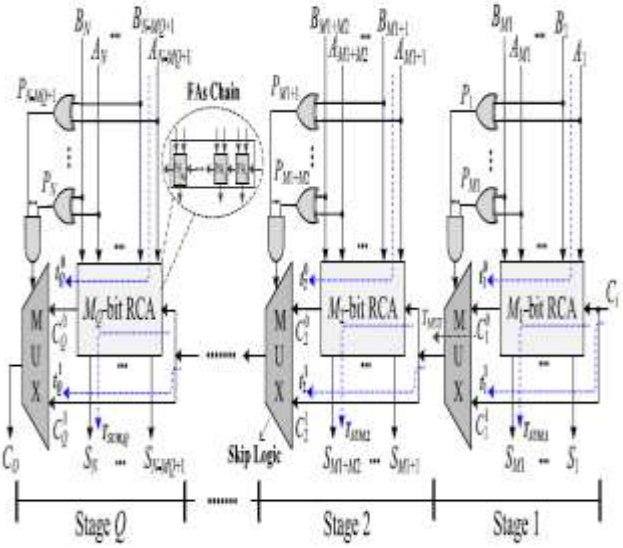

Fig .1: The conventional carry skip adder

The conventional structure of CSKA contains stages of full adders; Ripple carry adder (RCA) block and carry skip logic which contains 2:1 multiplexers. The RCA contains N cascaded stage of full adders; hence signal propagation delay is a sum of the two N bit inputs A and B. The worst condition path delay for this case is

Propagation delay Pi=Ai^Bi=1 ; i=1, 2……N

Where Pi indicates propagation delay of A.i and B.i, it indicates that RCA block delay is linearly propositional to N stage. If entire cascaded are in propagation mode then carry output is equal to carry input. Then skip logic indicates the present stage carry is ready for the next stage no need of waiting for the cascaded stage full adders operation [3].

B. Modified carry skip adder

This Modified carry skip adder is designed for further reduction propagation delay, the fig.2 shows the structure of Modified carry skip adder

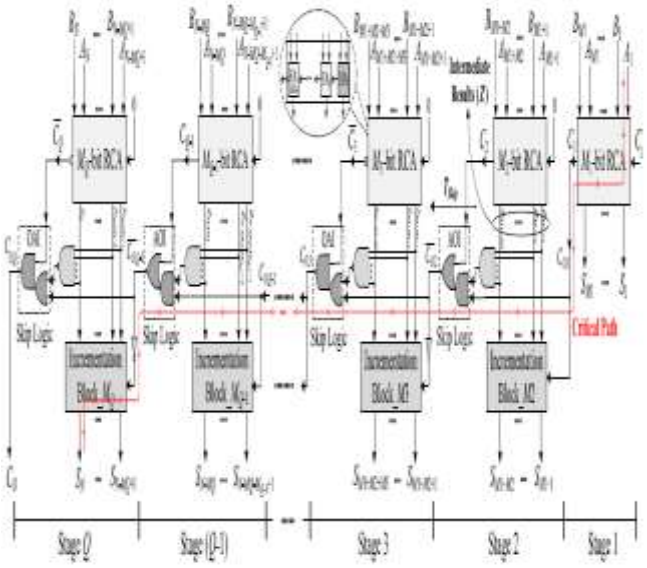

Fig.2 Modified carry skip adder

This structure contains Concatenation and Incrementation techniques with conventional CSKA. The skip logic contains multiplexer can be replaced by the AND-OR-Invert and OR-AND-Invert logic are used in skip logic instead of multiplexer; this skip logic gives inverting function of the gate. Hence inverting skip logic eliminates more power consumption and delay. In the above structure have only one block of RCA and then stage 2 to N is having two blocks of RCA and incrimination block [3].

C. Proposed Hybrid carry skip adder

This Modified carry skip adder is designed for further reduction propagation delay; the fig.3 shows the structure of Modified carry skip adder

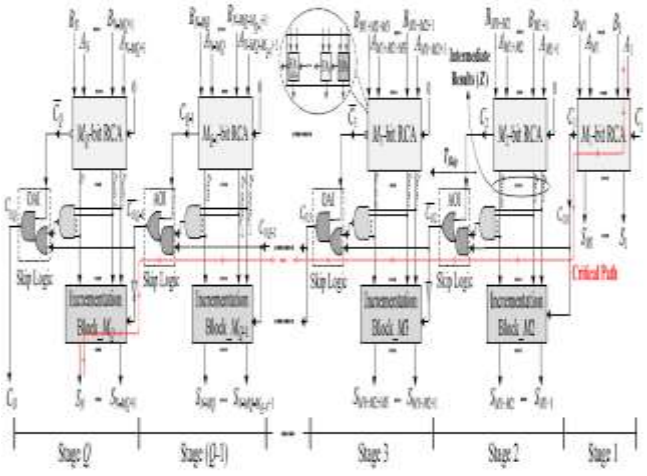

Fig .3 Modified carry skip adder

This structure contains Concatenation and Incrementation techniques with conventional CSKA. The skip logic contains multiplexer can be replaced by the AND-OR-Invert and OR-AND-Invert logic are used in skip logic instead of multiplexer, this skip logic gives inverting function of the gate. Hence inverting skip logic eliminates more power consumption and delay. In the above structure have only one block of RCA and then stage 2 to N is having two blocks of RCA and incrimination block [3].

D. Internal structure of Proposed Hybrid carry skip adder

The proposed Hybrid CSKA internal structure is as shown in the fig.4 contains modified PPA and skip logic with size of PPA network is 8 bit is as show in fig 3.4. This proposed hybrid CSKA as three stages are preprocessing level, PPA network and post processing level.

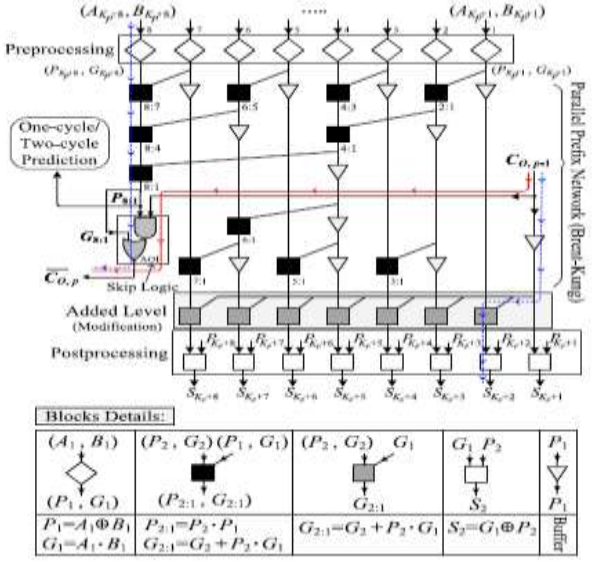

Fig .4 Proposed Hybrid CSKA internal structure

In preprocessing level, input signal propagating signal (Pi) and generated signal (Gi) are calculated. Next, Brent Kung network, the longest carry path signal G:8:1 of the network with P:8:1 is generated, which is summation of all propagation input signal are calculated faster than other intermediate stages signal of the network. For skip logic P:8:1 intermediate signal is used to find if carry output of previous stage is skipped or not. Here all these operations are done parallel with intermediate stages. If P:8:1 is 1 then C:o, p-1 stage should skip, indicating that critical paths are activated. If P:8:1 is 0 then C:o,p is equal to G:8:1 and stage indicating that no critical path is activated. In the post processing level, the final sum of output is calculated [2].

E. Kogge stone adder

The fastest parallel adder other than Brent Kung adder is Kogge-Stone adder because of its minimum fan-out but larger area is shown in fig.5. The operations of this adder is divided into three parts, they are Pre and post processing, look ahead network.

In a Preprocessing level, the propagate and generate signal are generated for a pair input bits A and B are

Pi=Ai ^ Bi

Gi=Ai & Bi

The carry look ahead stage separate Kogge-Stone network from others adder. It is the main reason for make this adder has more high performance adder.

This step produce carries for each bit and it uses group propagate and generates given by the equations,

Pi:j=Pi:k+1 AND Pk:j

Gi:j=Gi:k+1n OR (Pi:k+1 AND Gk:j

Sum bits are generated by using below equation,

Si=Pi XOR Ci-1

Kogge-Stone adder is most widely used adder because it will generates carry in O time. In most of the applications this adder is used for high performance.

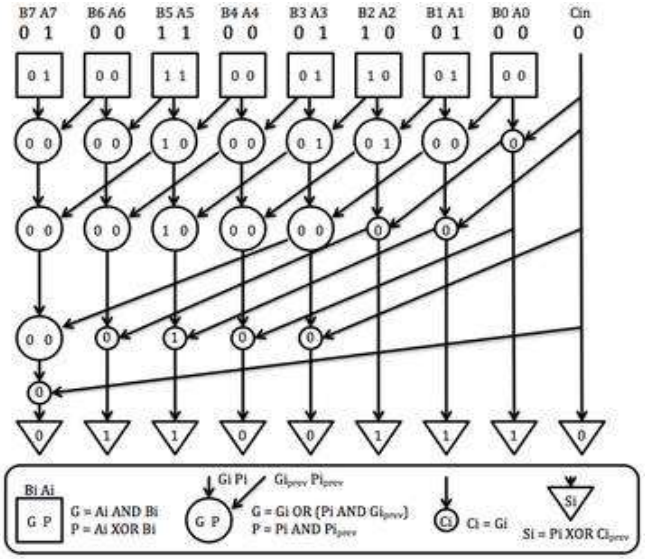

Fig.5 Kogge stone adders

F. Dual mode full adder (DMFA)

The name says dual mode full adder, it operated in two different modes they are Accurate and approximating mode. It is can able to switch both modes as per requirement, the Dual mode full adder as shown in the fig.6

In case, if 1 bit inputs are A, B and Cin of the full adder to DMFA, then B is the sum and A is cout. The proposed hybrid variable latency CSKA structure replaces all full adder cells by a Dual mode full adder cells, hence each Full adder can be operate either accurate mode or approximation mode depending on the Dual mode full adder control signal represented as APP. Let's assume, logic 1 to the APP signal indicates that the DMFA will be operating in the approximate mode and logic 0 to the APP signal indicates that the DMFA will be operating in the accurate mode. In addition, the full adder cell is power by VDD when it is in approximate mode.

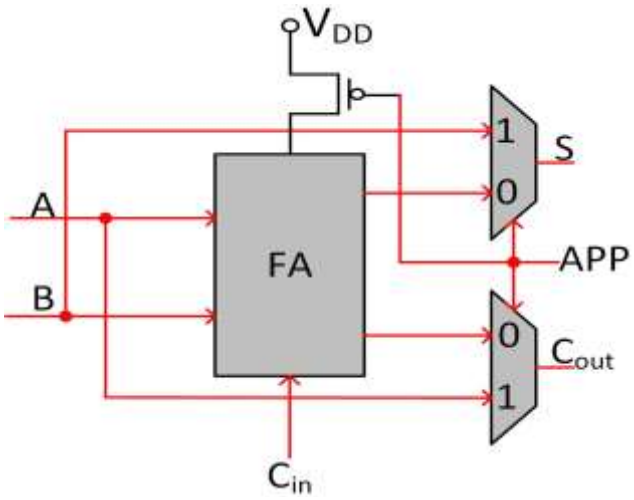

Fig.6 Dual mode full adder

The power consumption for a 16 bit Ripple carry adder is done in Synopsys tool and the obtained results are shown below.

Table-1: Different DMFA modes and their Power consumption

General full adder (µw)	DMFA in Accurate mode (µw)	DMFA in Approximation mode (µw)
1.53	1.74	0.01

The Table-1 results of the experiments show a negligible power consumption difference of the DMFA when it is operated either in both modes. Hence, approximation mode was chosen in proposed hybrid variable latency CSKA structure

The DMFA Overhead; in the figure 3.5 it shows power gated transistor and the DMFA multiplexer are used to provides a least overhead in cell. Table 3.1 shows the power taken by the full adder and DMFA in different. In the results, the power consumption rise by 0.21µ where it operates in accurate modes compared to full adder block. This mainly because of the more load capacitance of the full adder block due to the external input capacitance through the multiplexer's blocks in DMFA. Then small amount of additional power is contributed by the switching activity of the multiplexer's cell.

III. RESULTS

1) Conventional carry skip adder

The conventional CSKA front end design is carried out using Verilog coding and it is simulated by using Cadence NCSIM for 16 bit inputs as shown in fig.7 The RTL schematic for the synthesis results is as shown in fig.8

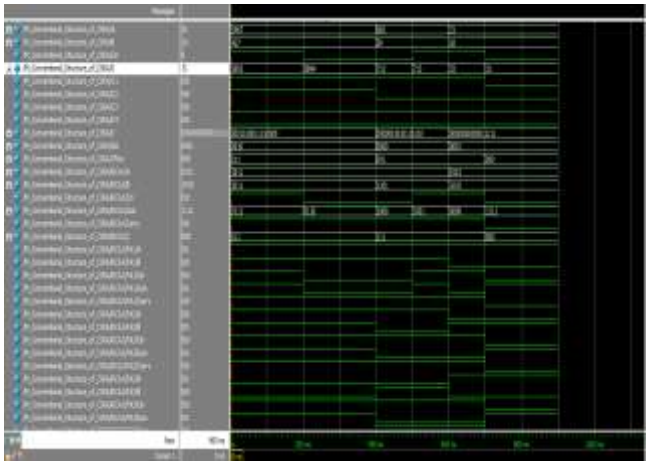

Fig.7 Simulation results of conventional carry skip adder

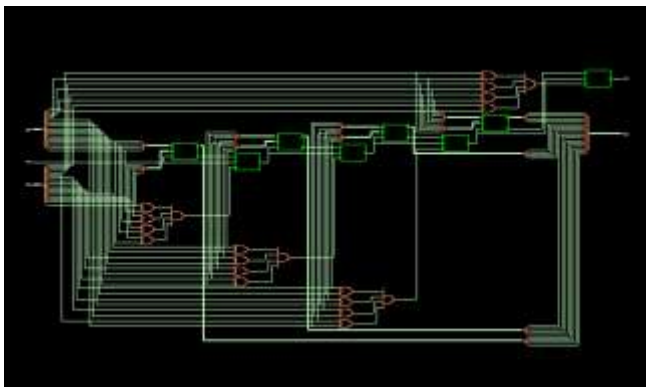

Fig.8 Synthesis RTL schematic of conventional CSKA

2. Modified carry skip adder

The Modified conventional carry skip adder contains additional incrimination and skips logic block compare to conventional CSKA. Based on skip logic output the next stage calculate carry out put sooner to propagate carry to the last stage, the front end design is carried out by using Verilog coding and it is simulated by using Cadence NCSIM for 16 bit inputs as shown in fig.9. The RTL schematic for the synthesis results are shows in a fig.10

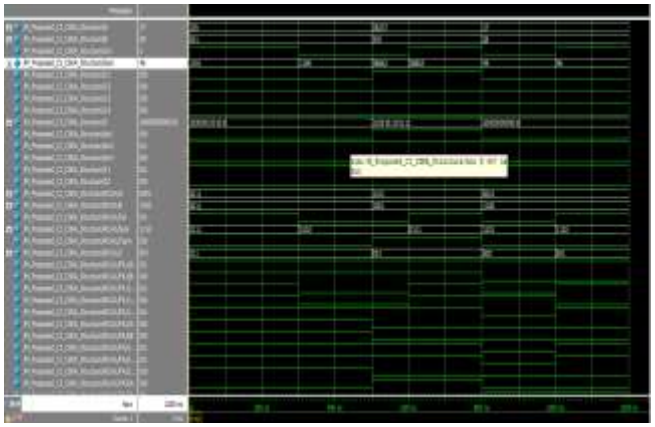

Fig.9 Simulated results of Modified carry skip adder

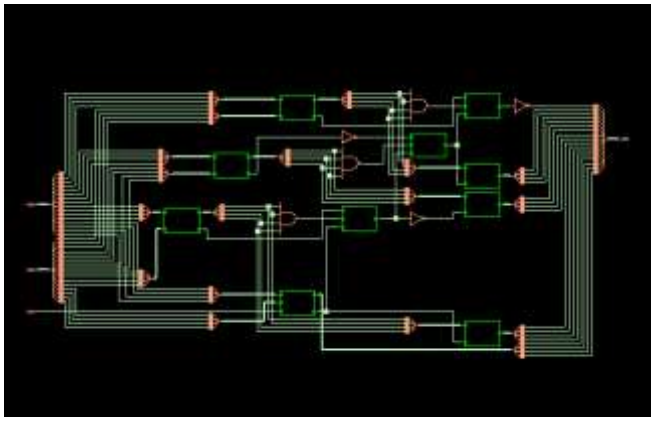

Fig.10 Synthesis RTL schematic of Modified carry skip adder

3. Proposed Hybrid carry skip adder using DMFA

The Proposed Hybrid CSKA using DMFA includes additional parallel prefix network called as Brent-kung adder, incrimination and skips logic block. This parallel prefix network is used because which speed up the operation and breaks the critical path delays. Its design is carried out by using Verilog coding and it is simulated by using Cadence NCSIM for 16 bit inputs as shown in fig.11 RTL schematic for the synthesis results are as shown in fig.12

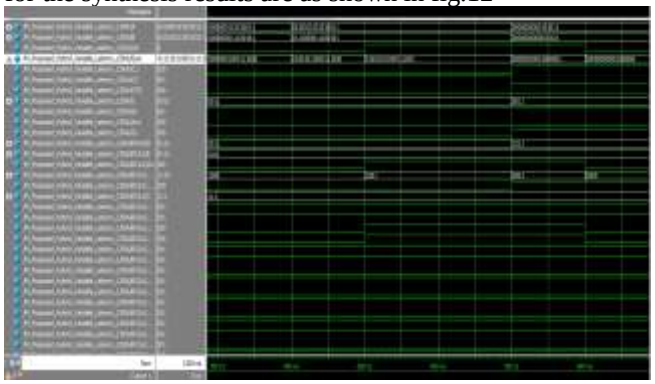

Fig.11 Simulation results of Hybrid CSKA using DMFA

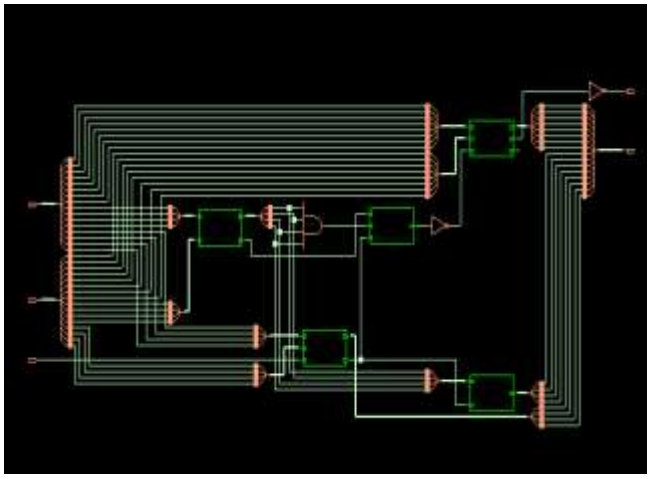

Fig.12 Synthesis RTL schematic of Hybrid CSKA using DMFA

4. Comparison of Power, delay and area

The conventional, modified and proposed hybrid CSKA is designed and synthesized by cadence encounter, the synthesized results shows power consumption, delay and area as shown in table-II.

Table-II: Power, area and delay for different architecture

Parameters	Conventional CSKA	Modified CSKA	Hybrid CSKA
Leakage power (nw)	69.035	53.210	50.007
Dynamic power (nw)	198816.37	192700.497	176371.72
Total power (µw)	198.88	192.53	176.421
Delay (ps)	2679	1165	1027
Area(µm)	1730	1543	1700

IV. CONCLUSION

The Hybrid CSKA was proposed, which shows high speed and less power utilization compared with conventional and modified structure. Enhancement of High speed is implemented by changing the structure called the concatenation and incrementation methods. Then skip logic is made by AOI and OAI logic which require fewer transistors than multiplexers. The efficiency of the hybrid structure is achieved by using PPA network and comparing PPA network power and delay with the conventional CSKA and modified CSKA.

Finally the RCA blocks are replaced with DMFA which consume less power. The power, area and timing reports also suggested that Hybrid-CSKA structure is better adder and it is suitable for applications where speed and energy consumption are critical.

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Santhosh N. S Lecture, Acharya Institutions, Bangalore. Area of interest is ASIC Design.

Shivarudraiah M.R Lecture, Acharya Institutions, Bangalore. Area of interest is ASIC Design.

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