Architecture of Static Random Access Memory Design Using 65nm Technology

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***Abstract*— For those headway in innovation organization and sort for Utilization of the hardware gadgets in distinctive applications, request Tremendous size memories will store alternately transform those information. Regularly static access memory (SRAM) cells would utilized because of its secondary Pace get to attributes. With the exponential increment in the Size of the memory, the force devoured Eventually perusing those memorycells would Likewise expanding exponentially. Reversible circuits clinched alongside later a considerable length of time. Have picked up its premium because of its low energy qualities. This Paper proposes Reversible SRAM cell with read and write signals. The recommended plan minimizes the number of trash outputs. Eventually perusing 66. 66%, Quantum expense by 71. 5% Also Quantum delay by. 68. 5% over the existing plans. . This paper additionally explains the execution points of interest of 16 × 8 SRAM array exhibit with minimum trash and quantum cost.**

***Index Terms*— Reversible Logic, SRAM Cell, TRASH Minimization and quantum cost**

I. INTRODUCTION

Low power VLSI configuration has picked up enthusiasm for late years due to its extensive variety of uses. Landauer has proposed that for each piece loss of data in consistent calculations that are not reversible, KT × ln2 Joules of vitality will be scattered as warmth, where K is the Boltzmanns consistent and T is the temperature in Kelvin at which the framework is working. Bennett demonstrated that zero power scattering in rationale circuits is conceivable just if a circuit is made out of reversible rationale entryways. The entryway which does not lose any data is called as reversible door. Reversible circuit has picked up its enthusiasm because of its minimization of nonadiabatic misfortunes which will diminish the warmth scattering . With the expansion in the memory application, outlining of low power memory cell has picked up enthusiasm for late years. A memory that comprises of circuits fit for holding their state the length of energy is connected is known as static recollections. Static arbitrary get to memory (SRAM) is well known among other memory cells because of its rapid qualities. SRAM employments a basic bistable circuit to hold an information bit. Two cross coupled inverters in the regular 6T cell shapes a lock which is utilized to store the information. At whatever point there is a requirement for putting away other information in a similar cell, past information must be deleted which demonstrates the irreversibility operation of the memory cell and brings about the warmth scattering. The calculations which take put in the customary memory are irreversible. Morrison et.al., has proposed SRAM configuration utilizing reversible circuit plan. Each door yield that is repetitive is known as waste yield. The principle challenge in the outline of reversible circuit is to lessen the refuse yield. A proficient SRAM cell is displayed in this paper with limited refuse yields, with limited quantum delay and limited quantum taken a toll as contrasted with the current outline . A 16 × 8 SRAM cluster was created with the proposed SRAM cell and with decoder.

Whatever is left of the paper is composed as takes after. Area II expounds writing Theoretical Background. Area III presents System Overview Segment IV delineate the System Analysis and Results and segment V presents conclusions.

II. THEORETICAL BACKGROUND

SRAM Basics

The memory circuit is said to be static if the stored data can be retained indefinitely, as long as the power supply is on, without any need for periodic refresh operation. The data storage cell, i.e., the one-bit memory cell in the static RAM arrays, invariably consists of a simple latch circuit with two stable operating points. Depending on the preserved state of the two inverter latch circuit, the data being held in the memory cell will be interpreted either as logic '**0**' or as logic '**1**'. To access the data contained in the memory cell via a bit line, we need atleast one switch, which is controlled by the corresponding word line

A. READ Operation

Consider a data read operation, shown in Figure 28.41, assuming that logic '**0**' is stored in the cell. The transistors M2 and M5 are turned off, while the transistors M1 and M6 operate in linear mode. Thus internal node voltages are **V1 = 0** and **V2 = VDD** before the cell access transistors are turned on. The active transistors at the beginning of data read operation

$$\frac{\beta_{N3}}{2}(V_{DD}-V_1-V_{TN})^2=\frac{\beta_{N1}}{2}(2(V_{DD}-V_{TN})V_1-V_1^2)$$

B. WRITE Operation

Consider the write '**0**' operation assuming that logic '**1**' is stored in the SRAM cell initially the voltage levels in the CMOS SRAM cell at the beginning of the data write operation. The transistors M1 and M6 are turned off, while M2 and M5 are operating in the linear mode. Thus the internal node voltage **V1 = VDD** and **V2 = 0** before the access transistors are turned on. The column voltage **Vb** is forced to '**0**' by the write circuitry.

$$\frac{\beta_{P5}}{\beta_{N3}}=\frac{\mu_P}{\mu_N}\cdot\frac{(W/L)_5}{(W/L)_3}<\frac{(2(V_{DD}-1.5V_{TN})V_{TN})}{(V_{DD}-V_{TP})}$$

Technology Scaling

Since the 1960's the price of one bit of semiconductor memory has dropped 100 million times and the trend

continues. The cost of a logic gate has undergone a similarly dramatic drop. This rapid price drop has stimulated new applications and semiconductor devices have improved the ways people carry out just about all human activities. The primary engine the powered the ascent of electronics is "miniaturization". By making the transistors and the interconnects smaller, more circuits can be fabricated on each silicon wafer and therefore each circuit becomes cheaper. Miniaturization has also been instrumental in the improvements in speed and power consumption.

Gordon Moore made an empirical observation in the 1960's that the number of devices on a chip doubles every 18 months or so. The "Moore's Law" is a succinct description of the persistent periodic increase in the level of miniaturization. Each time the minimum line width is reduced, we say that a new technology generation or technology node is introduced. Examples of technology generations are 0.18mm, 0.13mm, 90nm, 65nm, 45nm…generations. The numbers refer to the minimum metal line width. Poly-Si gate length may be smaller. At each new node, the various feature sizes of circuit layout, such as the size of contact holes, are 70% of the previous node. This practice of periodic size reduction is called scaling. Historically, a new technology node is introduced every three years or so. The main reward for introducing a new technology node is the reduction of circuit size by 2. (70% of previous line width means ~50% reduction in area, i.e. 0.7 x 0.7= 0.49.) Since nearly twice as many circuits can be fabricated on each wafer with each new technology node, the cost per circuit is reduced significantly. That is the engine that drives down the cost of ICs. Besides line width, some other parameters are also reduced with scaling such as the MOSFET gate oxide thickness and the power supply voltage. The reductions are chosen such that the transistor current density (Ion/W) increases with each new node. Also, the smaller transistors and shorter interconnects lead to smaller capacitances. Together, these changes cause the circuit delays to drop . Historically, integrated circuit speed has increased roughly 30% at each new technology node. Scaling does another good thing reducing capacitance and, especially, the power supply voltage is effective for lowering the power consumption. Thanks to the reduction in C and Vdd, power consumption per chip has increased only modestly per node in spite of the rise in switching frequency, f and (gasp) the doubling of transistors per chip at each technology node. If there had been no scaling, doing the job of a single PC microprocessor chip-- running 500M transistors at 2GHz using 1970 technology would require the electrical power output of a medium-size power generation plant.

III. System Overview

This section discusses the proposed SRAM cell design using reversible gates.The proposed fully reversible SRAM cell. Since the latch and the access transistors in the conventional SRAM is irreversible, latch and access transistors are modelled with the reversible elements.

A. Proposed Reversible SRAM cell

The Fredkin gate used as the access transistors. The inputs to the Fredkin gate are WL, previous data Fig.1: Proposed Reversible SRAM Cell The Fredkin gate used as the access transistors. The inputs to the Fredkin gate are WL, previous data, TABLE I: Truth table for access transistors during writing operation Bit(b) Word Line (WL) Data Stored (D)
X 0 Previous Data Stored
1 1 1
0 1 0
stored and bit (B) input. If WL = 0, third output will be the previously stored data. If WL = 1, third output will be the bit (B) input. During read operation the bit (B) and ¯ bit (¯B) of the SRAM cell is connected to the sense amplifier which is used to produce the corresponding output data. The latch was modelled by using one Feynman gate and one Fredkin gate. WL output in 3×3 Fredkin gate is used to enable the row cells. So, the total number of garbage output for the proposed SRAM cell is 1. Considering the line 2 in Figure 4 if WL = 0, data stored will be the output in line 2 of the 3 × 3 Fredkin gate which resembles the hold state of the access transistor. If WL = 1, data input will be the output of the line 2. This line 2 is fed to the Feynman gate which performs the latch operation.

B. Proposed SRAM cell with Read and Write Signals

This segment examines about the proposed reversible SRAM cell with read and compose signals. Figure 1 demonstrates the proposed reversible SRAM cell. A 3 × 3 Fredkin entryway and a 2 × 2 Feynman entryway is utilized to store the single piece of information and it is controlled by two 3 × 3 Fredkin entryway. Consider reality table for traditional SRAM cell as appeared in TableII. So,the contribution to the SRAM cell is word line motion from the push decoder, compose flag, information in, read flag and the yield of the SRAM cell is compose line which is passed to the following SRAM cell in a similar column, compose line, read line and information out.

The contribution to the 3 × 3 Fredkin entryways are compose flag, consistent info rationale "0" and the information input. The yield of the 3 × 3 Fredkin entryway are compose flag, rubbish and the yield line. At the point when WL = 1 , then the SRAM cell will be either in read mode or compose mode. In the event that compose flag is "1" then whatever the estimation of information in will be put away in the SRAM cell. In the event that the compose flag is "0" and if read flag is "1" then the esteem put away in the SRAM cell will be the estimation of the information out which looks like genuine usefulness of the regular SRAM cell. The quantum cost of the proposed SRAM cell with the read/compose flag is 16 and the refuse yield of the proposed configuration is 3. The plan is checked and reproduced utilizing Verilog HDL in Xilinx.

A. Proposed 16 × 8 SRAM Array

In this area, 16×8 SRAM cluster was proposed. The decoder is utilized to interpret the information address furthermore, is utilized to choose the proper word lines. The word line yield of each SRAM cell is utilized to empower the following SRAM cell there by decreasing the rubbish yield of each SRAM cell.The information was given by the compose circuits and the bit and bit of each SRAM cell is associated with the sense circuits in request to play out the read operation.In the proposed SRAM cluster, four 2-to-4 decoders are utilized with empower bit to interface eight reversible SRAM cells in an exhibit.

IV. System Analysis and Results

Rubbish yield minimization is one of the real undertakings in the outline of the reversible circuits.In this area, trash yield, quantum cost andquantum postponement of the current SRAM cell utilizing reversible circuit plan and the proposed SRAM cell is introduced. Table 1 demonsate the analysis of SRAM Design

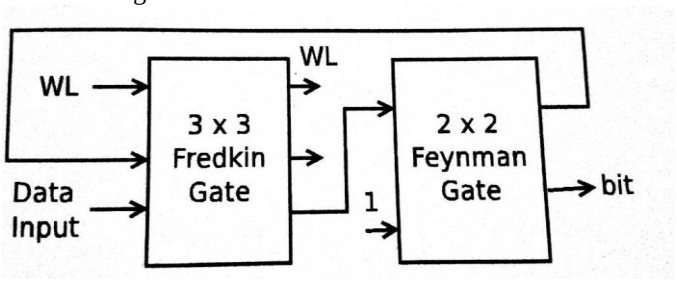

Figure 1:Proposed reversible SRAM Cell

V. Result

TABLE 1
Analysis of SRAM Design

Design	Parameter	Reversible Logic Implementation for Conventional Logic Design
SRAM	Leakage power (µW)	12559.613
CELL	Dynamic power (µW)	91676.525
DESIGN	Total power (µW)	101236.138
	Delay (ns)	22.485
	Area (µm²)	3683

µW= micro Watt, ns = nano second, µm= micro meter

VI. Conclusion

A novel SRAM cell was proposed and the cell was outlined with Fredkin and Feynman entryways. One Fredkin door and one Feynman entryways are utilized to outline the SRAM cell. In this way, the
add up to quantum cost of the proposed SRAM cell is 6 which is 71.5% lesser than the current outline of reversible SRAM cell. The most pessimistic scenario postponement of the proposed SRAM cell is 68.5% lesser than the current outline of SRAM cell utilizing reversible circuit plan [4]. The circuit was enhanced and the number of waste yields are diminished to 1 which is 66.66% lesser than the current reversible SRAM cell. The plan was confirmed utilizing Xilinx ISE test system and 16 × 8 SRAM cluster was executed with the decoder proposed.The reversible double substance addressable memory (BiCAM) and ternary substance addressable memory (TCAM) can be designedas an extension to this work.

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[12] J. A. Swanson, IBM Journal, 4, 305 (1960).We would like to take this opportunity to amplify two points in Swanson's paper which perhaps were not adequately stressed in the published version.

(1) The large number of particles (-100) in the optimum element are a result of the small energies per particle (or cell) involved in the typical cooperative phenomenon used in computer storage. There is no question that information can be stored in the position of a single particle, at room temperature, if the activation energy for its motion is sufficiently large (- several electron volts).

(2) Swanson's optimum volume is, generally, not very different from the common sense requirement on U, namely: vt exp(- U/kT)<<l, which would be found without the use of information theory. This indicates that the use of redundancy and complicated coding methods does not permit much additional information to be stored. It is obviously preferable to eliminate these complications, since by making each element only slightly larger than the "optimum" value, the element becomes reliable enough to carry information without the use of redundancy.

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