

Implementation of Five Level H-Bridge Inverter with Less Number of Switches and Reduced Harmonics

Pradeepa.K, Krishnan.S, Dhivyaa Dharshinii.M, Akshaya.S.R

Abstract--A multilevel inverter is a power electronic device that is used for high voltage and high power applications, with the added advantages of low switching stress and lower total harmonic distortion (THD), hence reducing the size and bulk of the passive filters. This paper proposes a new topology of a cascaded multilevel inverter that utilizes less number of switches than the conventional topology. Therefore with less number of switches in the circuit, there will be a reduction in the gate driver circuits and also in effect fewer switches will be conducting for specific intervals of time. The circuitry consists of smaller multilevel inverter blocks connected in series to achieve its characteristic output waveform. A five level inverter will be simulated and its effect on the harmonic spectrum will be analyzed. The system will be modelled with the help of MATLAB/SIMULINK.

In this paper a new topology of the cascaded multilevel inverter has been shown to produce an increased stepped output with less number of semiconductor switches. With fewer switches, controlling the overall circuit becomes less complex, the size and installation area reduces. Based on the simulation results there is a decrease in the overall THD.

Index Terms--Cascaded H-bridge multilevel inverter, Total Harmonic Distortion (THD).

I. INTRODUCTION

A multilevel inverter is a power electronic interface that Synthesizes a desired output voltage from several DC voltages as inputs. The research and development for these types of converters are gaining popularity especially for high power and high voltage applications due to the reduction in THD. Due to this the size of the passive filter will be smaller making the overall system compact. In addition to this, it produces output waveforms with a better harmonic spectrum, hence improved power quality and also has good electro-magnetic compatibility. Conventional multilevel inverters include diode clamped converter, flying capacitors, cascaded H-bridge. The cascaded H-bridge and the diode clamped are the most popularly hardware implemented topologies at present, especially in the growing technological field of renewable energy. Multilevel inverters have some disadvantages. One of the most obvious disadvantages is the numerous of power Semiconductor switches required. Every switch requires a gate driver circuit, therefore increasing the complexity and size of the overall circuit. The requirement of multiple gates Driver circuit leads to large expense; consequently in practical applications a reduction in the number of switches used is crucial. This paper presents a new topology of a cascaded multilevel inverter that has fewer semiconductor switches and gate driver circuits with higher number of steps in the output.

II. PROPOSED CIRCUIT

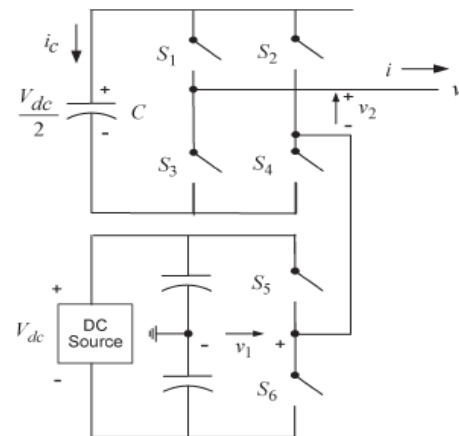
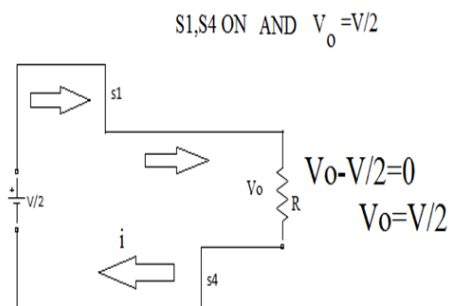


Figure 1.Single phase five level multilevel inverter for Proposed system

A. Proposed Circuit Operation

Mode 1 Operation

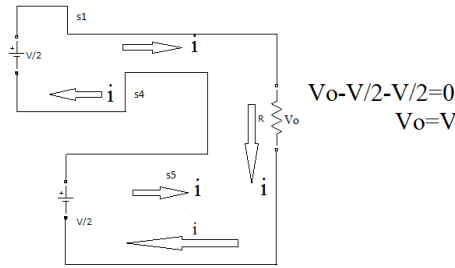
In the circuit two different voltage source are used for the below circuit the input potential is V and the above circuit input potential is V/2.To achieve the positive half voltage the switches S1 and S4 will conduct .The current start from voltage source and flow through the switch (S1) and through resistance and switch (S4) and end with the voltage source.



Mode 2 Operation

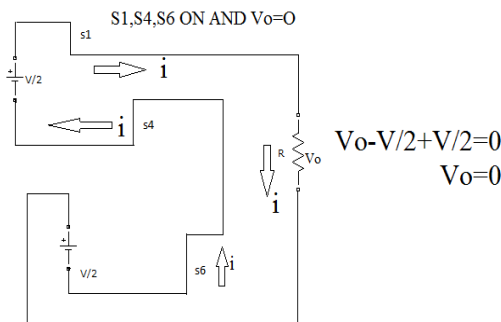
To achieve the positive peak voltage the switches S1, S4 and S5 will conduct. The current start from voltage source and flow through the switch (S1) and through resistance and switch (S4) and end with the voltage source.

S1,S4,S5 ON AND $V_o=V$



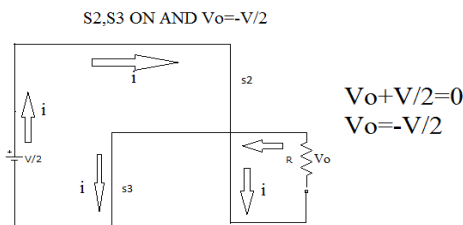
Mode 3 Operation

To achieve the zero voltage the switches S1, S4 and S6 will conduct. The current start from voltage source and flow through the switch (S1) and through resistance and flow through the voltage source and flow through the switch(S6) and flow through the switch (S4) end with the voltage source.



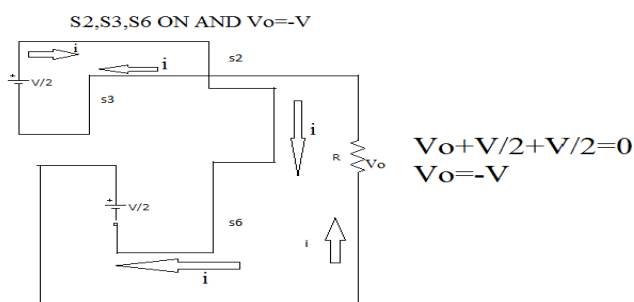
Mode 4 Operation

To achieve the negative half voltage the switches S2, S3 will conduct. The current start from voltage source and flow through the switch (S2) and through resistance and switch (S3) and end with the voltage source.



Mode 5 Operation

To achieve the negative peak voltage the switches S2, S3 and S6 will conduct. The current start from voltage source and flow through the switch (S2) and through resistance and flow through the voltage source and flow through the (S6) and end with the voltage source.



III. SIMULATION RESULTS

Simulation has become a very powerful tool on the industry application as well as in academics, nowadays. It is now essential for an electrical engineer to understand the concept of simulation and learn its use in various applications. Simulation is one of the best ways to study the system or circuit behavior without damaging it. The tools for doing the simulation in various fields are available in the market for engineering professionals. Many industries are spending a considerable amount of time and money in doing simulation before manufacturing their product. In most of the research and development (R&D) work, the simulation plays a very important role. Without simulation it is quiet impossible to proceed further. It should be noted that in Power electronics, computer simulation and a proof of concept hardware prototype in the laboratory are complimentary to each other. However computer simulation must not be considered as a substitute for hardware prototype. The objective of this chapter is to describe simulation of impedance source inverter with R, R-L and using mat lab tool.

Bridge inverter is called as H-Bridge Inverter. It is used to convert DC to AC. It is one type of Multilevel inverters. Cascade multi level inverter has the simple configuration compare than other multi level inverters. It is generate less harmonic and high level output voltage. Five level inverter shown in figure 6.has only six switches but conventional method require eight switches.

Simulation Circuit of Conventional Five Level H-Bridge Inverter for RL-Load

Figure 2.Shows the simulation circuit of conventional five Level H-Bridge inverter for RL-Load.

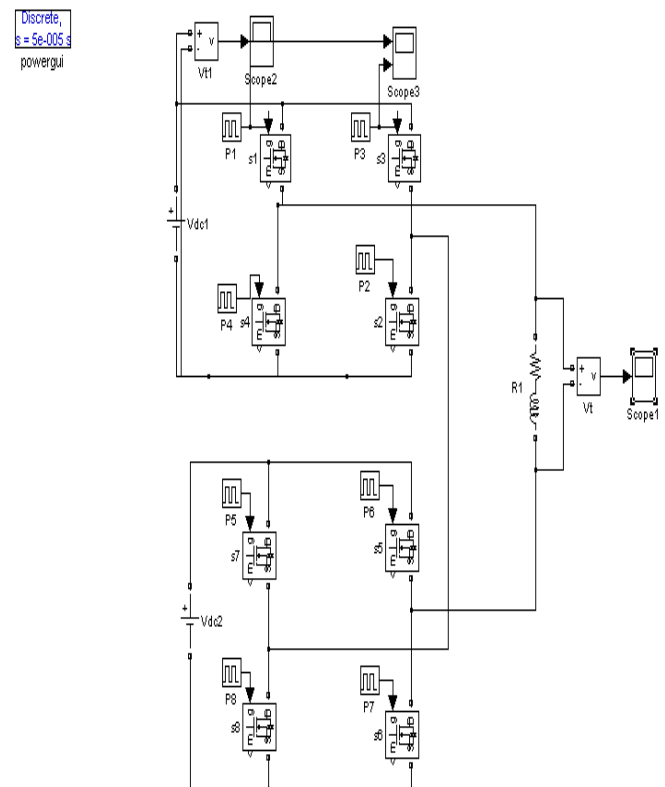


Figure 2.Simulation circuit of conventional Five level H-Bridge inverter for RL-Load

Input Voltage

Figure 3. Shows the DC Input voltage for the inverter Circuit

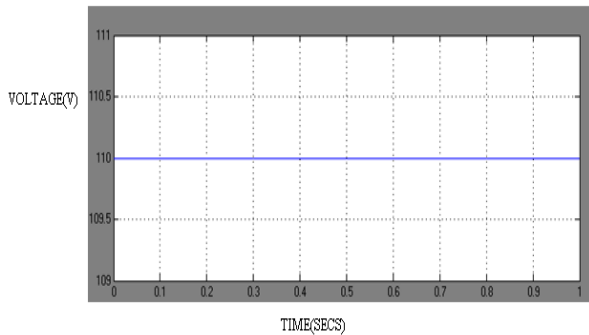


Figure 3. DC Input voltage for inverter Circuit

Output Voltage

Figure 4. Shows the output voltage across the RL- load.

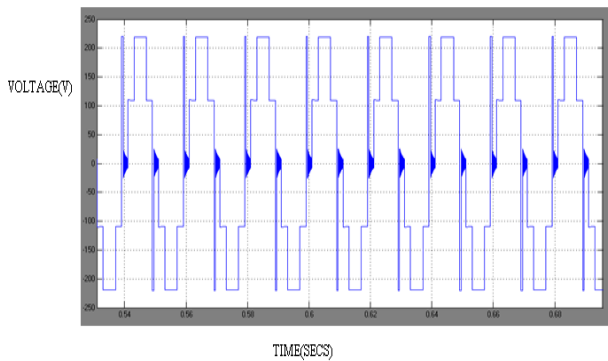


Figure 4. Output voltage across the RL-Load

FFT Analysis

Figure 5. Shows FFT analysis for conventional five levels H-Bridge inverter for RL Load was performed and the Total Harmonic Distortion (THD) was found to be 21.56% at the fundamental frequency 50 Hz

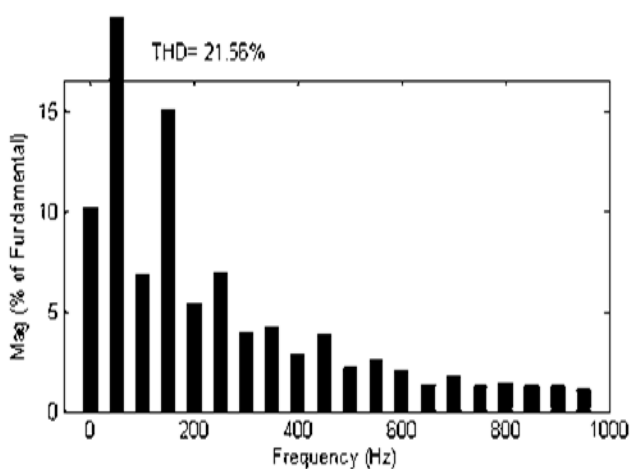


Figure 5. FFT analysis for conventional five level H-Bridge inverter for RL-Load

Simulation Circuit of Proposed Five Level H-Bridge Inverter for RL-Load

Figure 6. Shows the simulation circuit of proposed five Level H-bridge inverter for RL-Load.

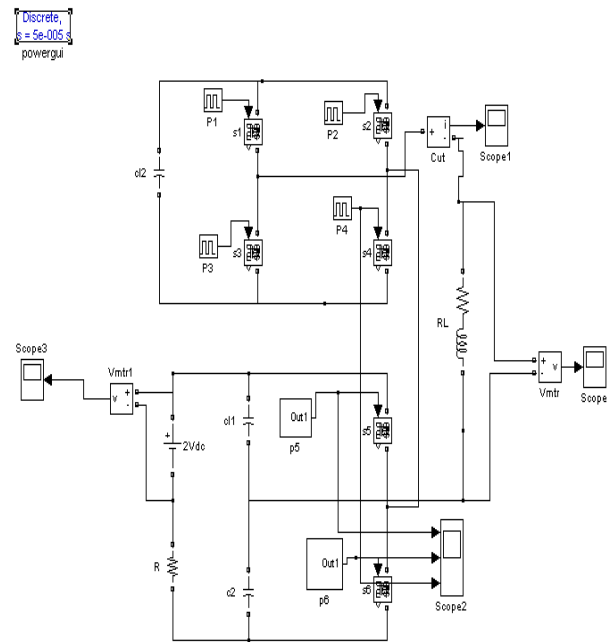


Figure 6. Simulation circuit of proposed five level H-bridge inverter for RL-Load

Input Voltage

Figure 7. Shows the DC Input voltage for the inverter circuit.

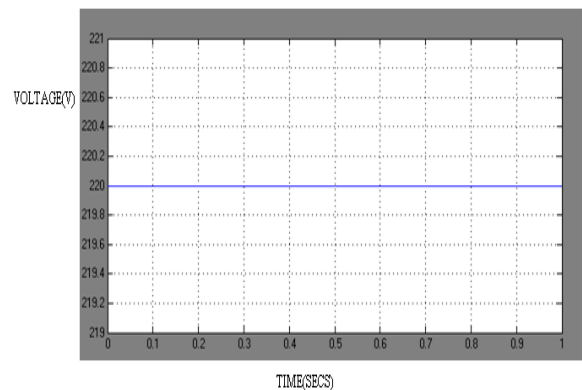


Figure 7. DC Input voltage for the inverter Circuit

Output Voltage

Figure 8. Shows the output voltage across the RL-load

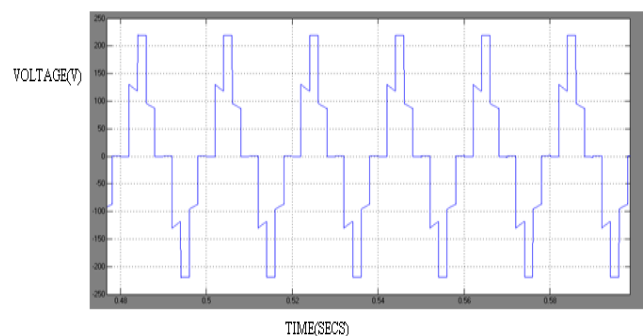


Figure 8. Output voltage across the RL Load

FFT Analysis

Figure 9 Shows FFT analysis for proposed five level H-Bridge inverter for RL Load was performed and the Total Harmonic Distortion (THD) was found to be 11.80% at the fundamental frequency 50 Hz

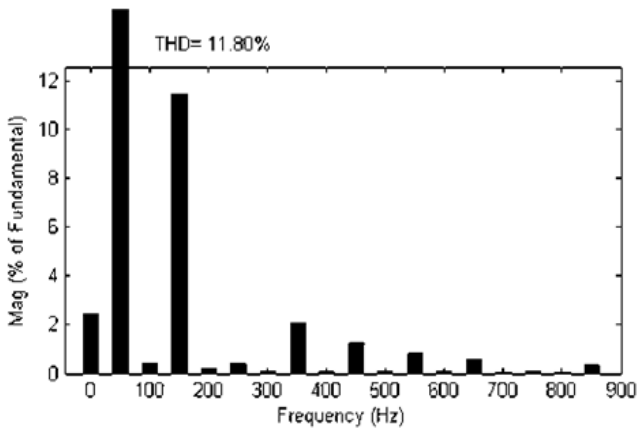


Figure 9. FFT analysis for proposed five level H-Bridge Inverter for RL-Load

TOTAL HARMONIC DISTORTION BETWEEN CONVENTIONAL AND PROPOSED FIVE-LEVEL MULTI LEVEL INVERTER

Table 1 shows that the Total harmonic distortion between conventional and proposed five level multilevel inverter.

FIVE LEVEL MULTI LEVEL INVERTER	TOTAL HARMONIC DISTORTION
Conventional Five Level Multilevel Inverter	21.56%
Proposed Five Level Multilevel Inverter	11.80%

IV. CONCLUSION

Thus a cascaded multilevel inverter that utilizes less number of switches was implemented. With fewer switches, controlling the overall circuit becomes less complex, the size and installation area reduces and there is a decrease in the overall THD. A five level inverter was simulated and its effect on the harmonic spectrum was analyzed. The system was simulated using MATLAB. The resulting system is used for high voltage and high power applications, with the added advantages of low switching stress and lower total harmonic distortion (THD), hence reducing the size and bulk of the passive filters.

REFERENCES

- [1] K. M. Rahman, N. R. Patel, T. G. Ward, J. M. Nagashima, F. Caricchi, and F. Crescimbeni, "Application of direct-drive wheel motor for fuel cell electric and hybrid electric vehicle propulsion system," IEEE Trans. Ind. Appl., vol. 42, no. 5, pp. 1185–1192, Sep./Oct. 2006.
- [2] M. Hinkkanen and J. Luomi, "Braking scheme for vector-controlled induction motor drives equipped with diode rectifier without braking resistor," IEEE Trans. Ind. Appl., vol. 42, no. 5, pp. 1257–1263, Sep./Oct. 2006.

- [3] C. H. Rivetta, A. Emadi, G. A. Williamson, R. Jayabalan, and B. Fahimi, "Analysis and control of a buck dc–dc converter operating with constant power load in sea and undersea vehicles," IEEE Trans. Ind. Appl., vol. 42, no. 2, pp. 559–572, Mar./Apr. 2006.
- [4] J. S. Lai and F. Z. Peng, "Multilevel converters—A new breed of power converters," IEEE Trans. Ind. Appl., vol. 32, no. 3, pp. 36–44, May/Jun. 1996.
- [5] J. S. Lai, J. Rodriguez, J. Lai, and F. Peng, "Multilevel inverters: A survey of topologies, controls and applications," IEEE Trans. Ind. Appl., vol. 49, no. 4, pp. 724–738, Aug. 2002.
- [6] L. M. Tolbert, F. Z. Peng, and T. G. Habetler, "Multilevel converters for large electric drives," IEEE Trans. Ind. Appl., vol. 35, no. 1, pp. 36–44, Jan./Feb. 1999.
- [7] C. B. Jacobina, E. C. dos Santos, M. B. de Rossiter Correa, and E. R. C. da Silva, "AC motor drives with a reduced number of switches and boost inductors," IEEE Trans. Ind. Appl., vol. 43, no. 1, pp. 30–39, Jan./Feb. 2007.
- [8] L. Ben-Brahim and S. Tadakuma, "A novel multilevel carrier-based PWM-control method for GTO inverter in low index modulation region," IEEE Trans. Ind. Appl., vol. 42, no. 1, pp. 121–127, Jan./Feb. 2006.
- [9] L. Schuch, C. Rech, H. L. Hey, H. A. Grudling, H. Pinheiro, and J. R. Pinheiro, "Analysis and design of a new high-efficiency bidirectional integrated ZVT PWM converter for dc-bus and battery-bank interface," IEEE Trans. Ind. Appl., vol. 42, no. 5, pp. 1321–1332, Sep./Oct. 2006.
- [10] M. Shen, J. Wang, A. Joseph, F. Z. Peng, L. M. Tolbert, and D. J. Adams, "Constant boost control of the Z-source inverter to minimize current ripple and voltage stress," IEEE Trans. Ind. Appl., vol. 42, no. 3, pp. 770–778, May/Jun. 2006.



Pradeepa.K/Assistant Professor, EEE department, Vel Tech, Chennai, India. Completed BE.,(EEE) in Rajalakshmi Engineering College, Chennai and ME., (PED) in S.K.R Engineering College, Chennai.



Krishnan.S/Assistant Professor, EEE department, Jaya Institute of Technology, Chennai, India. Completed BE.,(EEE) in T.J Institute of Technology, Chennai and ME.,(PED) in S.K.R Engineering College, Chennai.



Dhivyaa Dharshini.M /Assistant Professor, EEE department, Vel Tech, Chennai, India. Completed BE.,(EEE) in Vel Tech Multi Tech, Chennai and ME.,(PED) in Rajalakshmi Engineering College, Chennai.



Akshaya.S.R/Assistant Professor, EEE department, Vel Tech, Chennai, India. Completed BE.,(EEE) in Sriram Engineering College, Chennai and ME.,(PED) in Sri Venkateswara College of Engineering, Chennai.